

OCTOBER 2006

# SolidState

# TECHNOLOGY

*Celebrating our  
49th year*

THE INTERNATIONAL MAGAZINE FOR SEMICONDUCTOR MANUFACTURING

## Batch Furnace Radical Oxidation p. 39

- USJ Co-implantation p. 45
- Implant Patterning p. 53
- Photomask Optimization p. 58



[www.solid-state.com](http://www.solid-state.com)

# Using oxygen and hydroxyl radicals for batch-furnace oxidation

## EXECUTIVE OVERVIEW

Balancing the lifetime and residence time of radicals is critical to achieving acceptable radical oxidation growth rates and uniformities in large-batch reactors. Oxidation rates of silicon depend strongly on crystal orientation, resulting in difficulties when oxidizing device structures involving different silicon crystal surfaces, such as corners of shallow-trench-isolation (STI) and 3D transistors. This article describes the development of a radical oxidation process in batch furnaces that reduces the dependence of oxidation rates on the crystal orientation of silicon.

Conventional thermal oxidation produces high-quality oxides on (100) silicon surfaces but results in oxides with a higher amount of interface defects on (110) and (111) surfaces [1, 2]. As a result, most modern devices are manufactured using (100) silicon wafers. However, because electron mobility is the highest on the (100) surface along the  $\langle 110 \rangle$  direction and hole mobility is highest on (110) surfaces along the  $\langle 110 \rangle$  direction, there is an increasing interest in fabricating high performance CMOS devices on hybrid substrates with different crystal orientations [3]. New oxidation processes capable of producing high-quality and uniform gate oxides on both (100) and (110) silicon surfaces are necessary to enable this result.

Fabrication of 3D transistors for memory and logic devices also requires novel oxidation processes. As DRAM cell dimensions are scaled down, cell array transistors are changed from traditional planar transistors to recessed channel array transistors [4]. At technology nodes below 32nm, flash memories require FinFET transistors to boost drive current and reduce the short channel effect. For high-performance logic devices, FinFET and tri-gate transistors provide excellent opportunities for scaling devices beyond the 45nm node [5]. Nonplanar and multigate transistors demand uniform, high-quality gate oxides on 3D gate structures involving multiple silicon crystal orientations, which are challenging for conventional thermal oxidation tools.

beyond the 45nm node [5]. Nonplanar and multigate transistors demand uniform, high-quality gate oxides on 3D gate structures involving multiple silicon crystal orientations, which are challenging for conventional thermal oxidation tools.

T. Qiu, C. Porter, M. Mogaard, J. Bailey, H. Chatham, Aviza Technology Inc., Scotts Valley, California

For both dry and wet processes, oxidation of (110) silicon surfaces is significantly faster than that of (100) surfaces, ranging from 50% to 120% faster, depending on process temperature and film thickness.

The objective of this work is to reduce dependence of oxidation rates on crystal orientations to within 10%. Such processes have a broad range of applications, such as STI corner rounding, conformal STI liner, gate oxidation for 3D transistors, high-quality oxidation of polycrystalline silicon, and low-thermal budget oxidation of silicon nitride.

## Radical generation and distribution

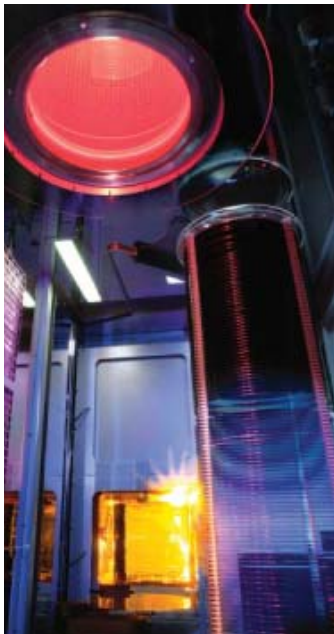
This work utilizes the hydrogen-oxygen combustion reaction to generate highly oxidizing radical species. To estimate optimum process conditions, the  $O_2/H_2$  reaction chemistry was simulated using a 22-step reaction mechanism derived from the H-O subset of a hydrocarbon combustion mechanism involving the intermediate species O, H, OH,  $HO_2$  and  $H_2O_2$  [6]. The reactions are evaluated using the chemistry simulation utility CHEMKIN [7] as well as a 3D flow and chemistry simulator. Computer simulations show that a significant amount of radicals can be created at 700°C and 1 torr and the radical lifetimes exceed 1 sec. At the oxygen-hydrogen ratio of 9:1, atomic hydrogen and oxygen are the dominating radicals, while the concentration of hydroxyl radicals is only 10% of the atomic oxygen.

Simulations show that the atomic oxygen number density is highly sensitive to the reaction temperature, pressure, residence time, and hydrogen-oxygen ratio. At lower pressures, the reactions are slower, and the radical lifetimes are increased. When the residence time of the radicals is comparable or longer than their lifetime, significant radical concentrations can be present in a reactor.

The reaction chemistry results were integrated into a 3D flow and chemistry simulation model to optimize hardware design and process conditions of a 300mm batch furnace by maximizing radical concentrations and lifetimes. **Figure 1** shows the predicted oxygen radical distribution over a 300mm wafer in a batch furnace at 700°C and 1 torr with a nitrogen-hydrogen-oxygen ratio of 10:1:1. The 300mm furnace was equipped with Aviza's patent pending Across-Flow technology.

## Characteristics of radical oxidation

A test reactor was built to verify the model predictions described above. The effects of pressure, temperature, and hydrogen-oxygen flow ratio on oxide growth rate were determined experimentally. **Figure 2** presents the effect of pressure on silicon oxidation at



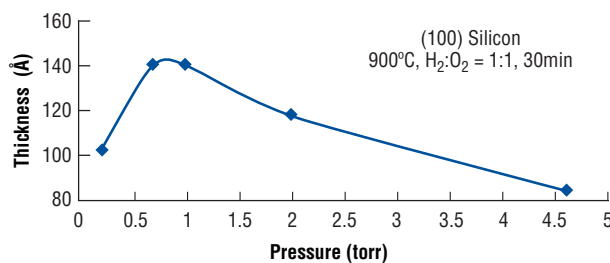


900°C and 1:1 hydrogen/oxygen ratio. The oxidation rate is maximized at ~0.9 torr. Below 0.7 torr, the oxidation rate drops with decreasing pressure, indicating that once the radical lifetime is sufficiently long, further reduction of pressure reduces the absolute number density of radicals and thus the oxidation rate. Above 1 torr, the oxidation rate decreases with increasing process pressure. This data suggests that at relatively high pressures, radical recombination is significantly increased and radical lifetime shortened, resulting in a net decrease of oxygen radicals despite the increased reactant number density. Overall, the experimental results confirmed the predictions of the simulations.

For comparison, low-pressure wet oxidation rates were also measured. Hydrogen and oxygen were converted into steam inside a catalytic steam generator prior to reaching the oxidation chamber. Steam was diluted with additional hydrogen and then introduced into the process chamber. **Table 1** compares oxides grown at 1 torr by both methods. At this pressure, wet oxidation is extremely slow, producing only a 1.8nm-thick oxide after 70 minutes of oxidation at 825°C. For radical oxidation, however, the presence of oxygen and hydroxyl radicals greatly increases the oxidation rate.

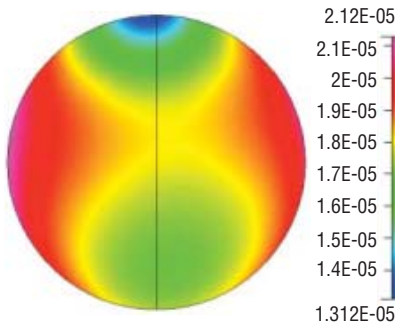
**Figure 3** presents growth kinetics for (100) silicon surfaces at 900°C and 700°C. The process pressure is 1 torr and the oxygen-hydrogen ratio is 1:1. The oxide growth shows a parabolic time dependence.

**Figure 4** presents the dependence of oxide thickness on crystal orientation for a series of seven 30-min. process conditions with varying temperature (700–900°C) and pressure (0.2–4.8 torr). The maximum oxide thickness difference between (100) and (110) surfaces ranges from the best case of 2.6% to the worst case of 18.5%, depending on process conditions and film thickness. This is a significant improvement compared to wet oxidation conducted at



**Figure 2.** Measured effect of process pressure on radical oxidation of (100) silicon. Experiments conducted in a test reactor.

Table 1. Radical oxidation vs. low-pressure wet oxidation at 1 torr				
Process	Temp. (°C)	Duration (min)	Chemicals	Oxide (Å)
Radical	700	30	O <sub>2</sub> :H <sub>2</sub> = 1:1	58
Steam	825	70	H <sub>2</sub> O:H <sub>2</sub> = 1:2.2	18



**Figure 1.** Calculated mass fraction distribution of oxygen radicals over a 300mm wafer in a batch reactor.

825°C and 588 torr with a steam-hydrogen ratio of 1:2.2. Wet oxidation creates oxides on the (110) surface 72–135% thicker than those on the (100) surface.

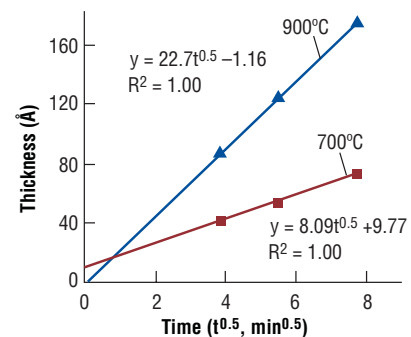
### Oxidation on batch furnaces

Process temperature was found to have a very weak impact on within-wafer uniformity and a strong effect on oxidation rates. Even at temperatures as low as 700°C, however, oxides <100Å can be grown within a reasonably short period of time. Variations of oxides grown on wafers of different crystal orientations within the same batch

are within 10%. Compared to wet oxidation at 825°C and 588 torr (**Table 2**), the sensitivity of the oxide growth rate on crystal orientation is reduced by a factor of 13.

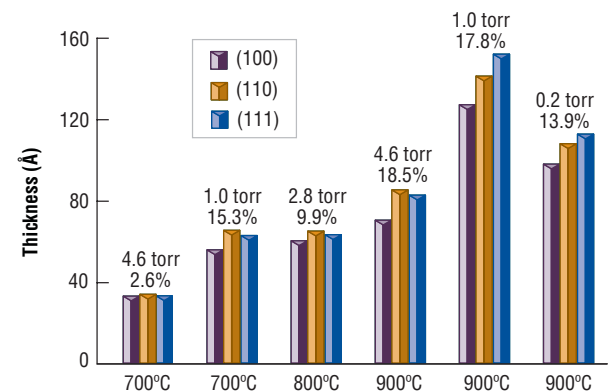
Current leakage characteristics for a 9.2nm thick oxide grown at 850°C using the H<sub>2</sub>/O<sub>2</sub> radical oxidation process were measured at five points on Si wafers using a mercury probe (area = 7.15×10<sup>-5</sup>cm<sup>2</sup>). The results are compared to data from a 9.6nm oxide grown by wet oxidation at 825°C. The oxide grown by radical oxidation shows superior electrical characteristics; leakage current remains low until about -8.5V versus -7V for the wet oxide.

Radical oxidation produces thin oxides with much better uniformity than conventional thermal oxides. **Figure 5** shows oxide thickness maps of top, middle, and bottom wafers in a 300mm large batch run at 900°C. The within-wafer-uniformity is within 1% (3σ). Compared to single-wafer hydrogen-oxygen combustion-based radical oxidation, the radical oxidation process using the method



**Figure 3.** Experimentally measured growth kinetics for radical oxidation at 900°C and 700°C.

continued on page 42

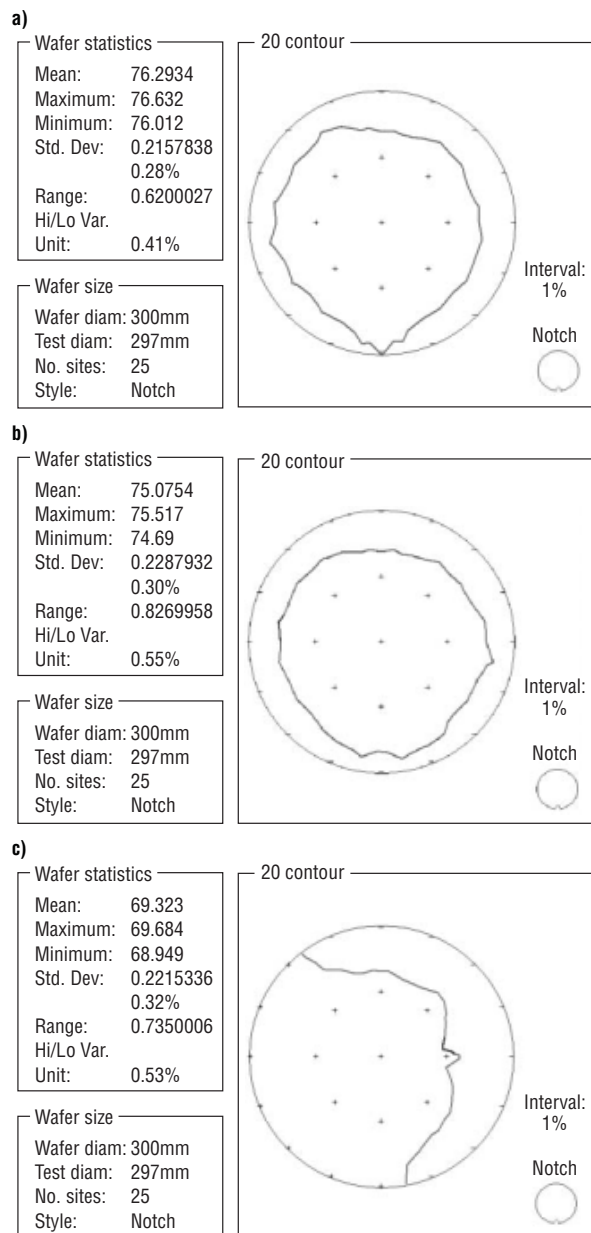


**Figure 4.** Measured radical oxidation oxide growth rates on (100), (110), and (111) Si. The percentage values are the maximum differences of oxides grown on the three different Si surfaces.

Batch-furnace radical oxidation continued from page 40

**Table 2. Thickness of oxides grown on wafers**

Time: wet oxidation Minutes	Thickness			Ratio	
	(100) Å	(110) Å	(111) Å	(110)/(100)	(111)/(100)
7	26.2	49.2	36.1	1.88	1.38
15	45.1	106	73.9	2.35	1.63
30	92.3	205	145	2.22	1.57
70	195	401	307	2.06	1.57
150	396	790	644	2.00	1.63
420	1000	1717	1536	1.72	1.54



**Figure 5.** Typical thickness uniformity of radical oxide films grown in a large 300mm batch furnace for wafers in a large wafer stack **a)** at the top; **b)** at the middle; and **c)** at the bottom.

described above achieves equivalent oxidation results while running at lower temperatures, lower pressures, and lower flows [8].

The lower thermal budget feature is beneficial for many applications, such as sidewall re-oxidation of transistor gates and gate oxidation for DRAM and flash memory. Lower oxidation temperature leads to reduced wafer heating and cooling times, in turn reducing process cycle time and increasing throughput. Lower hydrogen and oxygen flows reduce chemical cost. Combining these features with a large wafer batch size results in improved CoO over single-wafer tools.

## Conclusion

A computer simulation tool was developed to understand and optimize 3D radical generation and transport in batch reactors. Balancing the lifetime and residence time of radicals is critical to achieve acceptable radical oxidation growth rates and uniformities in large batch reactors.

Radical oxidation rates in a 300mm batch furnace were compared to experimental low-pressure wet oxidation. Oxidation of silicon by oxygen and hydroxyl radicals instead of steam greatly increases the oxidation rate and reduces the oxide thickness dependence on crystal orientation. Furnace radical oxidation also produces oxides with better electrical properties than wet oxidation. Batch radical oxidation can be applied in many advanced applications, such as base oxide for high-performance gate dielectrics, tunnel oxide for flash memory, gate oxide for DRAM transistors, fabrication of interpoly dielectrics for flash memory, and manufacturing of advanced STI structures. ■

## Acknowledgments

The authors would like to thank Helmuth Treichel for his counsel, Tom Fleming and Ed Guthrie for hardware support, and Billy Cho for equipment troubleshooting.

## References

1. R.R. Razouk, B.E. Deal, "Dependence of Interface State Density on Silicon Thermal Oxidation Process Variables," *J. Electrochem. Soc.*, 126, p. 1573, 1979.
2. S. Wolf, R.N. Tauber, *Silicon Processing for the VLSI Era, 1 - Process Technology*, p. 224, 1986.
3. M. Yang, M. Jeong, L. Shi, K. Chan, V. Chan, A. Chou, et al., "High Performance CMOS Fabricated on Hybrid Substrate with Different Crystal Orientations," *Tech. Digest of IEDM*, p. 453, 2003.
4. K. Kim, G.H. Koh, "Future Memory Technology Including Emerging New Memories," *24th International Conference on Microelectronics*, 1, p. 377, 2004.
5. S.E. Thompson, R.S. Chau, T. Ghani, K. Mistry, S. Tyagi, M.T. Bohr, "In Search of 'Forever,' Continued Transistor Scaling One New Material at a Time," *IEEE Trans. on Semiconductor Manufacturing*, 18, p. 26, 2005.
6. <http://maemail.ucsd.edu/combustion/cermech/>.
7. R.J. Kee, F.M. Rupley, J.A. Miller, M.E. Coltrin, J.F. Gracar, E. Meeks, et al., CHEMKIN Release 4.0.2., Reaction Design, San Diego, CA, 2005.
8. N. Sullivan, L.L. Raja, R.J. Kee, Y. Yokota, M. Williams, "Exploring ISSG Process Space," *9th Int. Conference on Advanced Thermal Processing of Semiconductors - RTP 2001*, p. 95, 2001.

**THOMAS QIU** is a principal research scientist at *Aviza Technology Inc.*, 440 Kings Village Road, Scotts Valley, CA 95066; ph 831/439-4326, e-mail [Thomas.Qiu@avizatechnology.com](mailto:Thomas.Qiu@avizatechnology.com).

At Aviza Technology Inc., **COLE PORTER** is a process development manager; **MARTIN MOGAARD** is a senior process development engineer; **JEFF BAILEY** is engineering R&D manager; and **HOOD CHATHAM** is a principal R&D engineer.